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Front-End Executive Outlook

Staff -- , 6/15/2004

As we look forward to the 65 and 45 nm technology nodes, challenges abound in virtually every aspect of the semiconductor industry. The push to smaller dimensions present challenges in lithography and maskmaking, as well as etch. The push to new materials to reduce time to market creates challenges with deposition, patterning, integration and inspection, as well as packaging. Automation continues to be important, not only in terms of optimizing yield and fab efficiency but also in terms of supply chain management. Equipment and materials suppliers, and their own sub-components and subsystems, are working to meet these challenges. For insight on these topics, *Semiconductor International* asked some of today's leading industry executives to give their outlook on what they're expecting to see at SEMICON West 2004. [Key trends in packaging](#) are also presented.

Lithography

Paul van Attekum
Senior Vice President of Marketing and Technology, ASML



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The long-awaited upturn in the semiconductor industry distinguishes SEMIC 2004 from its recent predecessors and provides a welcome backdrop for the see customers' need for "instant capacity" being met through the demand for lithography systems in both 200 and 300 mm wafer sizes. This trend will run throughout 2004. In the second half of this year, we also see increasing inter

sizes.

As semi-equipment manufacturers know, the fast migration toward new technologies require flexible solutions for customers. The newest member of ASML's TWINSCAN platform, the XT:1400, helps make my point. The system is a 0.93 NA, 193 nm scanner that images at 1 node for volume production and at the 45 nm node for process testing and development. It designed with the option of transitioning from "dry" to immersion lithography, giving custom flexibility to include immersion into their technology roadmaps while protecting their investment in 193 nm technology.

ASML believes customers should migrate to new technologies at their own pace, regardless of the state of the industry. This kind of flexibility will be increasingly important in the inevitable march toward more complex tools that perform at ever-smaller design rules.

Christopher Progler
CTO, [Photronics](#)



As industry momentum continues to build for volume production of 130 nm and 90 nm, we can forget the challenges encountered during yield learning for this node. The challenges have driven introspection in each member of the semiconductor product community from integrated device manufacturers to component, materials and suppliers. As a result, the march toward so-called manufacturability as a technical business imperative for future nodes is clear: Chip manufacturability drives yield and cycle time. Those that consider manufacturability in a real way during the technology development and prototyping process will lead into the next nodes.

The photomask fabrication process, from a manufacturability perspective, stands at a critical point between the chip design and physical manufacturing processes. In fact, the photomask is considered the first hardware realization of the overall design flow. Moreover, lithography productivity and, therefore, wafer yield are now intimately tied to the proper treatment of the photomask with resolution enhancement technology (RET). Finally, in a properly designed wafer fab, lithography is typically the rate-limiting step for wafer output, and photomask fabrication often gates the lithography cycle time for new design releases. Considering these points, proper integration of photomask data preparation and fabrication into the design flow is fundamental to achieving manufacturability in new design releases. Fully optimal integration of the photomask into next-generation design flows will require advances in many facets of the infrastructure, including verification methods, data transfer models, simulation tools, content generation and prototyping. However, the benefits of such activities will have industry-wide impact and, for nodes beyond 130 nm, are mandatory for chip manufacturability.

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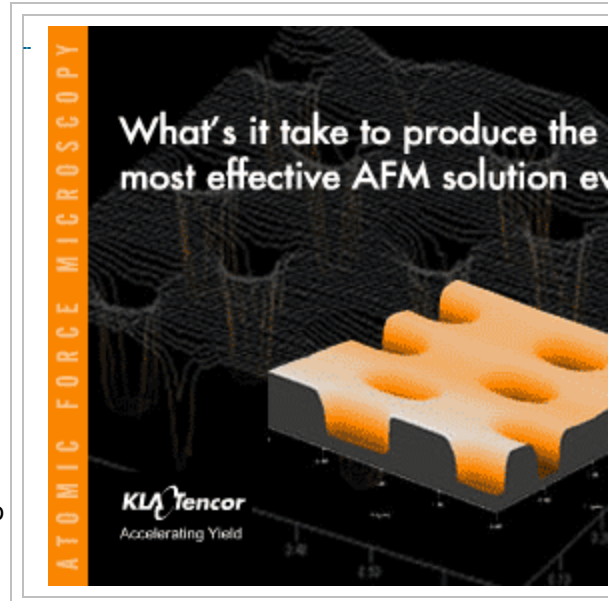
General industry trends

John Voltz
Vice President of Sales and Marketing, Genus Inc.



Without a doubt, atomic layer deposition (ALD) continues to be an enabling technology for both IC and thin-film head manufacturers.

ALD will be the foremost topic discussed in our booth at SEMICON West; however, the technologists who are looking for ALD films are already working with us for advanced solutions (the same scenario holds for advanced lithography, etch, etc.).



When it comes to major wafer processing disciplines, there are few if any process engineers or large device makers walking around a SEMICON show looking for new solutions. Today's semiconductor industry is moving too quickly, and we as suppliers need to know what the solutions are years before the tools are actually required. The major equipment suppliers in the industry know where the greenfield fabs are, and what they need from us. The 30,000-wafer-starts-per-month fabs don't just sneak up on you. We see them on the horizon years before any orders are placed.

For us, the content and value of SEMICON shows have changed. First of all, booth foot traffic in the few years has been weighted more toward visits from analysts, venture capital groups and investors rather than actual customers. We hope that changes this year with the equipment market heating up in most segments. The analysts are assessing the growth potential in our sector and the industry overall; today's SEMICON definitely provides us with the opportunity to have informal meetings with the investment community. For partnerships with other suppliers, SEMICON provides a lot of discussion because it always brings together a critical mass of the right people. For partnerships that began at recent SEMICON shows have gone on to be significant in our product development cycle.

I believe we are seeing the concept of SEMICON starting to change. While there are some new product launches, there is more emphasis on events like user group meetings, company- and process-specific technical seminars, panel discussions and other meaningful dialogue-oriented events, rather than the classic focus on booths and equipment. It's just a question of where you choose to spend your marketing dollars, and most companies today need to make sure they are focused directly at the customer.

Bill Gately
General Manager, Philips AMS



It appears from all accounts that 2004 is really the beginning of the next semiconductor market upturn. However, in many aspects, this upturn is very different than its predecessors. This upturn lacks the big killer app that drives technology acceleration across a wide range of chips. It lacks the step function type sharp expansion and equipment purchases that the previous upturns exhibited. A prevailing mood of cautious optimism and risk aversion that was absent in the technology-driven good old days. This is evidenced by the fact that we routinely talk to fab foundries that are running at capacity utilizations of 90% and over, and they are still cautiously adding capacity. And this is at the beginning of the upturn! In short, the industry has matured

This maturity has resulted in a shift to a more operationally focused strategy for most chip makers. They are focused on manufacturing excellence to build profit margins, since premium pricing is difficult to achieve today. This means that decisions on capital equipment purchases are now more heavily weighted by cost of ownership factors such as throughput, reliability and ease of use rather than technological capability. Today, semiconductor equipment, particularly metrology, must have compelling cost of ownership numbers to be selected for use in a high-volume fab. This presents challenges to many of the previous market-leading capital equipment companies that have based their product development strategies on leading-edge technology alone. It does, however, create an opportunity for the emergence of new leaders that have developed products from the beginning with this strategy in mind.

Jerry Cutini
President and CEO, Aviza Technology



The growth and digital convergence occurring in the global electronic end markets will drive our business continue to propel demand for faster, smaller and less expensive semiconductors. Computing, communications, consumer and automotive markets will continue to evolve into more sophisticated arenas. Mobile computing solutions, integration of voice, Internet, video and photo capabilities in cellular handsets, embedded systems in vehicles, and the smart global consumer's need for the complete "digital experience" will continue to drive the semiconductor industry marching forward with Moore's Law. Keeping up with this pace requires the continuous improvement (in cost, cycle time and performance) of all modern ICs such as microprocessors, flash memory and digital signal processors produced by IDMs, foundries and "fab-lite" companies.

It is the equipment industry that enables this march forward, providing the technology that allows our customers to keep pace with Moore's Law. To help our customers to continually deliver improved performance, the semiconductor equipment industry must continue to advance overall tool and process performance.

This year's SEMICON West will reflect these improved end markets and the updated business and technology dynamics that have come as a result of the economic challenges of the past few years combined with geopolitical landscape changes and technology challenges associated with subwavelength semiconductor manufacturing. The industry upturn, manufacturing economic recovery, operational streamlining and strategic outsourcing will address the business dynamics of a market being defined by industry and economic observers as a maturing industry.

China will again be a strong area of focus, as this region is rapidly establishing itself as the global IC producing region. The continued migration to 300 mm wafer manufacturing and 90 nm below design rules will keep our technical community lively as new challenges require the use of novel dielectric, metal and composite materials aimed at achieving optimum process integration. The material evolutions of the past, show attendees and exhibitors will discuss adoption of new process technologies, such as atomic layer deposition, which is expected to be one of the growing areas in the equipment sector over the next several years. The trends taking place in the era of nanotechnology will also continue to drive the need for increased industry consolidation, collaboration/partnerships and technology breakthroughs throughout the electronics value chain.

All of these topics will garner strong interest from what has become an increasingly diverse group of IC makers, equipment makers, investors, and Wall Street and industry researchers who will be attending this international gathering.

Jeff Bruchez
Director, Semiconductor Equipment Assessment (SEA)



In this post-recessionary period (however long or short), topics that support the International Technology Roadmap for Semiconductors (ITRS) and Moore's Law predictions will be evident, as equipment and material companies seek to attract interest in their products. Topics related to foreseeable nanoCMOS technology nodes down to 45 nm and related process applications (e.g., low-k and copper for interconnect, high-k for gate stacks) will obviously be present.

However, not all companies are solely driven by such quests. The equipment and material sectors are mainly comprised of small to medium enterprises (<250 employees and turnover <\$100M) seeking a more predictable return on investment in the nearer term while also seeking alternative products. Accordingly, a phased and balanced approach is required to both short-term equipment requirements and longer-term R&D and their intended uses. Applications will also include "diversions" away from mainstream nanoCMOS into implementation of "added value" process technologies at mature technology nodes (e.g., advanced substrates, special layers for vision products, photoresist devices, integrated MEMS, magnetic materials for non-volatile memory and advanced sensors) where added functionality can be achieved more cost-effectively and quickly by users.

Ultimately, the implementation of progressive nanoCMOS technology nodes and derivatives will be driven by performance, but by cost and proof that the new material technologies are robust, and reliable when integrated into process schemes that have also matured with proven circuit architectures. This can only be achieved via cooperative ventures/alliances, and increasingly occurring rather than sooner, often being deferred to later technology nodes. Accordingly, issues such as throughput, equipment reliability, cost-effectiveness, automation and APC/analysis/metrology will feature increasingly at SEMICON, as will the ability to effectively address a variety of applications at shorter-term production nodes (90 to 65 nm). R&D results for the longer term (e.g., 45 nm and beyond) will be prevalent mainly to attract initial user interest.

Joe Cestari
President, ILS Technology



At SEMICON West this year, you will see engineers looking for turnkey process solutions associated with strained silicon, silicon germanium and SOI. Leading manufacturers have clearly indicated that these three areas are in line to play in driving the industry at the 90 nm node. Beyond just process solutions, not yet effectively addressed turnkey solutions of transportation, in-fab delivery, and abatement for the toxic and corrosive chemistries involved. In fact, even with processing in use today, there is still a need for better precursor and abatement management.

Supply chain and cost of business will also be a topic of conversation, particularly at the Supply Chain Conference in San Jose. Our industry is definitely at the "must do" threshold our collective buying power and drive standardization on pre-competitive materials. We need the discussion from the theoretical to the practical and identify opportunities to get costs of business; equipment costs are still higher than they should be. The overall challenge for this is to produce packaged die at prices that the market is willing to bear.

Another hot area involves everything surrounding hardware and software for process and equipment control. Here, the IC manufacturing industry is at another critical threshold. The extension of Moore's Law depends on the industry effectively developing and agreeing to the needed standards and moving forward with APC, AEC and e-diagnostics. But there are still a lot of disparate efforts in the supplier community that make it difficult for fabs to succeed with these disciplines. This has to change. As an industry, we need to improve our participation and support in the standards being driven by SEMI and International SEMATECH.

Ludo Deferm
Vice President, Business Development, IMEC

Today, the semiconductor industry is facing one of the most difficult periods in its history, particularly driven by the 2001 ITRS. Material layers and transistor structures will soon reach their ultimate performance limits, preventing a reliable and efficient performance of the transistors and their interconnections. Large breakthroughs are needed to surpass this red brick wall, and to continue the success of the industry as such.

The continuous evolution toward more global technology partnerships forces generic technology development to be carried out in R&D collaboration schemes in which intellectual property is shared among the participants, without endangering each partner's IP portfolio for their product development.

Technology trends

Mark Pinto
Senior Vice President, Applied Materials



Significant changes continue in our industry, driven by the goal of achieving cost advantages and functionality improvements via higher levels of integrative scaling. However, the 65 nm and beyond technology nodes present challenges considerably more difficult than the ones we've encountered in the past, requiring integration of new materials and increased precision and control.

In the interconnect area, extremely narrow structures, low-k dielectric materials, and the increasing number of metal layers are driving advances in processing technologies, with emphasis on process control and cost of ownership. A good example of how the industry is addressing these challenges is through advances in CMP. CMP of the copper/low-k structures is affected by many factors: copper overburden topography, low-k material composition and film pattern density, costly consumables, and so on. While much progress has been made in reducing polishing head downforce to manage the shear force applied to low-k films and to control dielectric erosion, the development of "soft" or non-contact removal techniques shows great potential to simultaneously achieve superior planarity, protect delicate dielectric layers, and reduce copper requirements. Novel techniques to clean and dry hydrophilic (copper) and hydrophobic (low-k) surfaces after CMP are also being introduced to control defect levels. Innovations in these areas, such as electrochemical polishing, can take us to at least the 45 nm generation, and probably beyond.

In transistor scaling, the industry is actively pursuing technologies that address the key power dissipation. This power "crisis" is forcing the industry to redefine today's gate formation processes. Going forward, the industry must implement new materials like high-k dielectrics and innovative metal gate materials like dual metal alloys to leverage smaller CET (capacitance equivalent thickness) and yield higher, optimized drive currents with higher speeds. Techniques like plasma nitridation, which can enable tenfold improvements in leakage reduction over thermal nitride, are being adopted. In addition to advancements in the gate, substrates are also changing, with selection of SOI technology to combat power dissipation by mitigating leakage and capacitance. Other approaches, such as inducing strained silicon, or modifying the source/drain, will enhance NMOS performance. Further drive current improvements can be gained with ultrashallow junction (USJ) work, where recent technology developments enhance junction depth and allow resistivity scaling to continue.

Future technologies that move the industry beyond 65 nm will continue to be increasingly complex. Early integration of processes during equipment development plays a critical role in rapidly accelerating the introduction of new materials and processes. We will also need a much more collaborative approach to solving the complex issues of future chip generations by enhancing relationships between chip designers, equipment suppliers and chipmakers to enable manufacturable products while minimizing risks.

Robert B. MacKnight
Vice President and COO, Mattson Technology Inc.



The 45 nm technology node poses several technical challenges. In the front end of line (FEOL), the transistor gate length will have to be shrunk to $\leq 18\text{ nm}$, and the source/drain extension will have an ultrashallow junction (USJ) depth of <math>< 12\text{ nm}</math>. High-k dielectrics and metal gate will be needed for the transistor. The contact material will have to switch to NiSi with thickness $\leq 20\text{ nm}$, yet low sheet resistance must be maintained. To enhance the channel mobility, a new strained silicon technology may have to be developed.

implemented. Bulk silicon device architecture may have to be replaced by fully depleted SiC such as a 3-D finFET. These challenges not only put more thermal budget constraints on FEOL processes, but also have strong impact on BEOL technology in both the FEOL and back-end (BEOL) regimes. Thermal budget constraints may be overcome by established RTP techniques and derivatives, such as a millisecond anneal.

In the strip area, challenges include the need to maintain integrity of the gate, USJ and sili contact during photoresist strip. Silicon loss from the source/drain regions must be avoided high-dose ion implantation strip (HDIS). The exposure of NiSi during post-contact photoresist also must not create surface damage, which would increase the contact resistance. The critical dimension of the gate length has to be preserved by preventing the metal loss from the gate. These mandate the use of non-aggressive, novel chemistries during the photoresist strip.

At the 45 nm node, the BEOL processes employ ultralow-k (ULK) dielectrics (k~2.2) in the dual-damascene structures. Post-ULK plasma strip will have a strong impact on the dielectric integrity. Hence, it is critical to prevent oxidation of methyl groups in ULK by using new photoresist chemistries during plasma strip. If fluorocarbon-based resist is required for advanced lithography, fluorine-scavenging strip chemistries may need to be developed to preserve both gate and dielectric integrity.

Louis Steen
Vice President of Marketing, Tokyo Electron America



Traditional silicon-based materials, such as SiO₂ or polysilicon, have performed many generations. But scaling to atomic dimensions raises fundamental issues that require use of truly new materials and their integration into structures that were concepts just a few years ago.

These are exciting challenges, but they're risky. So development resources are shared to lessen the risk to any one party. Consortia and other pre-competitive projects are underway to decide among the multiple options available. These projects have many sponsors and the information will be widely shared among participants. Venues for this type of work include Nanotech (where TEL has its new TEL Technology Center at Albany), International SEMATECH, and IMEC. Other projects will be in the customers' critical path to manufacturing, and will involve both chip manufacturer and supplier. We are doing an increasing number of both types of projects and expect to see many other alliances announced during SEMICON West.

Once materials and structures have been selected, they must be assembled to atomic tolerances, day after day in manufacturing. This is where integrated metrology (IM) becomes critical. By measuring what our tools actually produce, then using this information on the tool or up/downstream, we can more reliably meet the tightest tolerances, and increase fab yields. With IM, chipmakers can manufacture structures for the 65 nm node and beyond. While metrology has been at the show for many years, I believe that IM is finally beginning to show its value in high-volume manufacturing. I expect to see the tool suppliers focusing on this technology.

Bill Moffat
CEO, Yield Engineering Systems Inc.

This year, the technology trends for copper and low-k dielectric treatment lead us into a new

exciting era for the semiconductor industry.

IBM has done some very interesting work developing and moving into production a process that deposits a thin amino silane layer as a trench copper diffusion barrier. They have reported that this layer is as effective as 200 Å of tantalum or TaN. As linewidths continue to decrease to 100 nm below, we think the potential for reducing conductor resistivity and heat generation with thin diffusion barriers that allow conductor cross section to increase from 600 to 960 Å is very great. A combination system with vacuum copper anneal also allows the removal of unwanted voids. Perfect treatment of the surrounding low-k dielectric will be welcomed by the industry.

Silane deposition may also play a role in increasing surface hydrophobicity of porous low-k to repair resistivity degradation by water intrusion.

We see a potential for integrating controlled-atmosphere copper anneal, conformal vapor silicon diffusion barrier deposition, porous dielectric surface treatment, and organic low-k dielectric deposition in the same tool set. For the future, copper annealing, low-k dielectric treatment, capping, and repair of plasma-damaged low-k dielectric can be done in one piece of equipment.

Michael Chase

Director of Marketing, Varian Semiconductor Equipment Associates Inc.



As the industry transitions from 90 nm to 65 and 45 nm, there are likely to be significant changes in the doping space, in particular in the ultrashallow junction well formation areas.

In the case of shallow junction formation, implant energies for the source/drain extension (SDE) are dropping to the sub-keV range and are reaching levels as low as 200 eV for the p-type junction. Because of space charge limitations, it is difficult to transport high beam currents to the wafer at very low energies. Since high beam currents are required for high throughput, this is creating a productivity bottleneck in the high-volume manufacturing of advanced scaled devices.

Semiconductor manufacturers are attacking this problem with three different approaches. One approach is to switch from boron to BF₂ as the dopant species for p-SDE applications. BF₂ junction depths equivalent to those with boron at ~5x the energy required for boron. The high mass of the BF₂ allows for higher beam currents and hence an increase in throughput.

Adopting decel-mode operation is an alternative approach. In this operating mode, the dopant is extracted from the ion source at a higher energy, and then decelerated to the desired energy before the beam reaches the wafer. This approach results in higher beam currents at the wafer by extracting the beam at very low energies. Depending on the sensitivity of the device, to use decel-mode operation, process and integration engineers may need to make minor changes in their process to allow for the small amounts of energy contamination that occur in decel-mode operation.

The third and emerging approach is to consider plasma doping as an alternative to beamline implanters for high-dose, low-energy applications. Plasma doping systems in general are not current limited, even at very low energies. Applications running 15-25 wph on a beamline hi dose system can run at 50 wph and higher on a plasma doping system.

In the case of well formation, there are also likely to be significant changes. Implant energy requirements are dropping such that the majority of the well steps can be performed on a medium-current ion implanter for the majority of logic applications. This is good news for semiconductor manufacturers, since medium-current ion implanters typically cost less, have smaller footprints, and have higher throughput. Furthermore, SOI applications do not require any high-energy implants because the insulating oxide layer supplants the need for implanted wells. Applications such as deep wells for certain memory segments, flash and CCD will continue to require high-energy implants.

Wilbert van den Hoek

CTO and Executive Vice President of Integration and Advanced Development, Nov Systems Inc.



As the industry shifts to 65 nm geometries, there are a number of technologies that are likely to be highlighted at this year's SEMICON West.

One of the most pressing issues facing semiconductor manufacturers today is how to extend process technologies. With device geometries shrinking ever more rapidly, suppliers must provide cost-effective and innovative production solutions that can shorten the learning curve for the development of next-generation tools and technologies.

Another likely topic of discussion at SEMICON West will be the integration of low-k dielectrics. With much of the industry now focused on high-mechanical-strength films, the key is to move beyond resist poisoning, via stress migration and electromigration, and instead focus on process integration issues that may arise in the back end. The development at Novellus of compressed (k=3.0) organosilicate glass (OSG) films is a major breakthrough enabling the use of conventional low-cost packaging technology for chips that contain low-k films. Since packaging has been recognized as a critical area, collaboration between semiconductor equipment and leading-packaging manufacturers is necessary to improve the strength of the interconnect structure.

Ivo J. Raaijmakers

CTO and Director of R&D, ASM International NV, Front-End Operations

In the 2003 ITRS, near-term challenges for the interconnect structure of microprocessors include: (1) the introduction of new materials to decrease the RC time constant; (2) the defect-free manufacturing of an interconnect structure with these new materials; and (3) the control of the interconnect structure in three dimensions.

The introduction of new materials in high-volume IC production has been a traditionally slow process, taking generally more than 10 years after the first application-oriented publications. Not surprisingly, this is also the case for low-k dielectrics. The 2001 ITRS (very optimistically!) called for a new generation of low-k materials for every technology node; this is not happening in reality. In the 2003 ITRS, realism has replaced optimism, and the introduction of porous ultralow-k materials is being scaled down. Minimizing the attainable effective k value by using extensions of the current non-porous dielectrics used in 90 nm HVM (perhaps with a slight scaling of material properties) and increasing the proportion of low-k material in the entire stack is an alternative path.

The reductions in bulk k value and the optimization of the stack structure for effective k value will surely result in a reduction of the overall mechanical strength of the dielectric stack. Soon

the availability of low-impact CMP will therefore become a sine-qua-non for defect-free manufacturing of the entire interconnects. The key challenge is to develop such low-impact copper deposition and removal technologies that can result in within-die and die-to-die planarity of $<500 \text{ \AA}$, so that dimensions of the interconnect structure are managed within tight tolerances in three dimensions independent of chip design.

Last but not least, ALD and plasma-enhanced ALD barriers are now being developed by everyone in the field. The University of Helsinki and ASM Microchemistry have pioneered application of barrier materials since 1995. ALD barriers have now been shown to lower line resistance (by maximizing the amount of low-resistance copper in the trench) and via resistance (by minimizing amount of higher-resistance barrier material in the via bottom). The perfect step coverage of ALD barriers make them ideal in the defect-free lining of (ultra-)low-k structures. Considering the time it takes from first publications to first high-volume manufacturing, one would expect that the industry will start to see ALD barriers in high-volume production fairly soon.

Phil Blakey

President, Semiconductor Business, North America, BOC Edwards



Processing technology: Atomic layer deposition (ALD) process development offering unique potential to meet some of the challenges of critical process steps required to meet or exceed the ITRS. The rate of maturation of the requisite technology, and supporting equipment and materials and delivery systems, is limited by the new demands presented by this processing technique. Gas in-vapor delivery systems as well as pumping and abatement systems need to be adapted to these new requirements, and additional cooperative effort is required to keep up with the needs and wants of the ALD process engineer. This year's SEMICON West show will continue to highlight the critical alliances that need to exist between equipment manufacturers and suppliers to improve the production-worthiness of the various commercial system offerings.

Cleaning technology: The most likely injection point of supercritical CO_2 (SCCO_2) technology in well-publicized applications in residue removal and low-k repair is thought to have moved to the next node. In the meantime, it is likely that post-implant and post-etch photoresist removal, as well as critical drying applications in high-volume MEMS production, will embrace SCCO_2 for its unique enabling capabilities. SEMICON West 2004 is a likely venue for announcements relevant to the formation of commercial alliances between tool suppliers, materials and subsystem providers; the addition of significant new players to the field is unlikely.

Electronic materials: The importance of fluorine-based materials for chamber cleaning in both device and flat-panel display processing moved to the point-of-use fluorine generator technology to the next stage during the last SEMICON West show. While the use of fluorine itself — as opposed to SF_6 — is cost-effective, it has profound implications for pump design and exhaust abatement. At the 2004 SEMICON show, we expect to see BEOL product offerings from several suppliers to complement the increasing adoption of fluorine generator technology into robust integrated

Materials

Saket Chadda

CTO, Honeywell Electronic Materials



As SEMICON West 2004 approaches, we are once again experiencing a time in the semiconductor industry. The ability to sustain this growth is not just a supply and demand; it will be driven by continued innovation and development. SEMICON West provides a great opportunity to meet with a variety of people in the industry and address some of the details around the latest developments. As a leading supplier of electronic materials to the semiconductor industry, I believe there are a number of interesting key points and trends in the materials arena, and look forward to discussions about these topics at the show.

Among them is the projected use of ALD for gate dielectrics (65 nm) as well as for back-end applications (barrier) at the 45 nm node. Further, the use of spin-on materials to accomplish 65 nm shallow trench isolation (STI) applications and the potential use of ruthenium as a barrier in addition to a thin layer of tantalum for direct plating (65 nm) proves interesting. Continuing the debate over the implementation of low-k materials progresses, it appears that device makers are using CVD low-k dielectrics for 90 nm and below, and this use is projected to continue, but with concerns about porosity at 65 nm. Moreover, in this area, we should see the use of materials to replenish carbon in low-k films post-etch/ash. Finally, aluminum may be headed for a comeback at 45 nm and because of its lower resistance.

As an industry, we've spent a lot of time focusing on numbers associated with the last downturn. Just as we can count on a cyclical growth path, we can also count on innovation and development. This year, as always, we'll have a lot to talk about.

André-Jacques Auberton-Hervé
CEO, Soitec



As the leading supplier of SOI, Soitec is well placed to observe the dichotomy between the aspirations of the industry as we prepare for future technology nodes, and as we supply current demand. This push-me/pull-you tendency in our industry is thoroughly manifested at the upcoming SEMICON West.

In many ways, the industry seems to think that 65 nm is already there, so that the work of the engineers and the work in R&D are already focused on 45 nm. This will be a hot topic at SEMICON West. But if you look at the reality of the industry, most manufacturers are still trailing behind 90 nm. The 130 nm node has just reached maturity.

Those of us on the leading edge of the materials industry are seeing an acceleration in the development of new materials — not just growth in demand, but an expansion into different kinds of materials. This demonstrates that there is no single road to scaling. Innovation in engineered substrates and widely advanced materials reflect a greater focus on transistor structure, bringing silicon materials performance and front-end technologies back to the forefront.

And finally, as a wafer supplier, we perceive that 200 mm continues to thrive. While investments in 300 mm are certainly the ones driving the industry, 200 mm investments are moving in parallel. It's coming down to design size: If the chip isn't very big, it currently does not justify a move to 300 mm. So for now, scaling will continue in parallel for both 200 and 300 mm wafers. Innovation will continue to drive 200 mm fabs toward longer lifetimes and higher profitability.

Chuck Kummeth
General Manager, 3M Electronics Markets Materials Division



Semiconductor manufacturers face a myriad of technical challenges, including manufacturing 300 mm wafers, transitioning to copper interconnects, implementing low-k dielectrics, and producing ultrathin wafers. While industry roadmaps have identified solutions for the immediate technical challenges, the semiconductor industry is counting on innovation from leading material suppliers to meet long-range challenges. These include the continuing need to help their customers speed time to market, reduce their total cost of ownership, address yield and reliability issues, and ensure that the huge investments required to stay competitive are worth the risk. Suppliers that can do this by offering customers easier access to a broad range of technologies and services become more valuable than ever before.

For example, there is an increasing demand for material suppliers to offer a higher level of capabilities. The growth of chip production in areas of the world such as China is one trend that manufacturers' need to know that, wherever they do business, they can count on their suppliers. Companies that can match their global strengths to those of their customers will continue to grow along with the industry.

Another trend is the need for IC companies to consider the environmental impact of their products throughout their life cycle. Companies have done an excellent job of reducing the environmental impact of their manufacturing processes. For example, significant reductions in greenhouse gas emissions have been achieved through the use of environmentally sustainable materials. However, the total impact of their operations — from raw materials through disposal or recycling — is still a significant challenge.

Finally, there is a growing reliance on technology and material innovation to improve chip performance and wafer yields. To achieve this, suppliers require a deep understanding of chip manufacturing processes and products to develop and design materials that enable the industry roadmap. Methodologies such as "design for six sigma" help ensure that the voice of the customer is embedded in the development cycle. This understanding of their customers' challenges will enable companies to develop solutions to the "big issues" for the industry — now and into the future.

Thomas H. Cook
Global Industry Executive Director, Dow Corning



We are definitely seeing an increase in demand for new CVD precursor materials as the first generation of low-k and copper barrier films move into production at the 65 nm technology node. Our read from the industry is that CVD-based low-k technologies will continue to be extended to the 65 nm technology node, and likely the 45 nm node as well. There is a great deal of activity already focused on developing the second generation of CVD precursor materials targeted in the 2.4-2.6 range for dielectric constant. While porous dielectric materials with $k < 2.4$ have been demonstrated, they are a long way from achieving the integration performance that is required for the cost-effective, high-volume manufacture of IC devices.

Dow Corning was one of the first companies specifically developing materials targeted for low-k back in the early 1990s. Low-k material development has been a tough road to follow, and we have learned to adapt along the way. We have been fortunate to get wins in both the spin-on area with silsesquioxane-based products and, more recently, in the low-k CVD precursor area. Most companies will never pay back their investments in low-k material development, which is unfortunate for the material supplier community, since it tends to stifle future development efforts. We expect to see companies looking for new ways to partner to address the material challenges that exist in the industry today.

Christopher Detrick
POU Commercial Manager, SAES Pure Gas Inc.



Over the past few years, the semiconductor industry has experienced a huge correction. This has offered many companies the opportunity to develop the next-generation devices and to shrink the geometries of current devices. 157 nm lithography is becoming common talk in the industry, and new technologies are taking us into uncharted territory with 45 and 32 nm node development along with nanotechnologies penetrating the industry. 300 mm wafer fabs are becoming the norm. Where filtration was a concern in the past to remove particles from a gas stream, today the particles that are inherently in a process gas and not removed by a filter are becoming the problem. Common gas impurities include H₂O, O₂, CO, CO₂, hydrocarbons and others. We have seen an increase in gas purification throughout the industry worldwide.

Gas purifiers can remove these impurities down into the parts-per-trillion range on most of the gases used today. Removing these impurities has been proven to increase yield and the final product reliability. Removing moisture from corrosive gas has proven to reduce downtime on equipment. The cost to replace valves, flow meters and other components that are affected by the acid when moisture is present.

Gas purity continues to be a critical issue for increasing yield, improving the process, reducing equipment downtime and controlling contamination. With the diversity of applications requiring purification, it is important to choose the correct purification technology for each specific application.

Eric Johnson
COO, JSR Micro Inc.

While we all have become accustomed to the continuous flow of technological breakthroughs to advance the pre-ordained roadmap defined by Moore's Law, the 45 nm node presents significant new challenges in not only science but also approach. The pressure on materials to provide the impetus for this advancement has been discussed often. As significant, however, is the requirement for integration of these materials not only within a given process, but across what previously were considered relatively independent activities.

Cross-process integration pressure is not a new issue for some applications. CMP has confronted integration issues as it has been expanded into new processes. Development work with low-k dielectrics, however, provides an excellent example of the new realities of significant increased integration needs. Formerly specialized process areas — lithography, etch, interconnect and even packaging, which has historically remained isolated from front-end manufacturing, now longer function as individual silos.

Material suppliers have a unique perspective on these integration issues. The breadth of materials we have in development and the depth of technical understanding necessary to work with our customers across various processes often enable us to identify and address potential integration roadblocks in our manufacturing processes. Success at the 45 nm node will thus depend on the deepening of the joint effort between the material suppliers and IC manufacturers.

As we continue to reduce critical dimensions and work toward 45 nm, process integration is becoming increasingly critical. To make 45 nm a success, we must have a clear technical awareness throughout the entire manufacturing process and understand the need for material science disciplines that historically have been treated as isolated activities.

Alan G. Knapp
Vice President, Microelectronics and Strategic Accounts, USFilter



Water is often referred to as the world's "universal solvent" and its "lifeblood." Without water, neither the human race nor the world as we know it would exist without it. As with our lifeblood, industries rely on this precious liquid for everything from cooling to power generation to manufacturing. There is no end to how this universal solvent is applied.

The microelectronics industry is no different, with the need for ultrapure water and unique water treatment requirements. Without water and the treatment technologies available, current microelectronics manufacturing yields could not be achieved. Current forecasts on geometry will require innovative water treatment technologies to meet the needs of future production.

Ultrapure treatment has matured with proven process techniques. In addition, water specific technologies have come a long way since the late 1970s, when processor requirements were measured in parts-per-million. The industry has pushed purification requirements to parts-per-trillion detection limits as geometries move into nanometer line widths. To put this into context, the geometry is comparable in size to human DNA.

Although it is not as important to the manufacturing process, many semiconductor fabs find wastewater treatment challenging, as facility byproducts must be treated to protect the environment. Processing techniques are tending toward using more diversified elements in the periodic table, such as copper, ammonia, hydrogen peroxide and other proprietary slurry solutions, which challenge the wastewater treatment industry to develop state-of-the-art technologies. As the microchip geometry and processing techniques continue to evolve, so too will the challenge to apply safe, effective and economical treatment techniques.

Proven treatment technologies along with innovative treatment processes will be merged to produce high-quality ultrapure water for manufacturing while treating the waste stream to protect our environment. After all, water is our lifeblood.

Standards

Stephen Knight
Director, Office of Microelectronics Programs, National Institute of Standards and Technology



Measurements are organic to semiconductor manufacturing and fundamental to the future. The latest ITRS lists more than 100 measurement-related milestones to be achieved if the industry is to continue its incredible — yet almost formulaic — success in squeezing ever more devices on a chip. For more than half of the metrology challenges, there are no known solutions for achieving the levels of accuracy and precision that will be required on the fab floor by 2009, when the industry is transitioning to the 45 nm node. Given the many challenges, it should not be surprising that industry spending for measurement-related equipment and operations has been increasing at an estimated annual rate of 15%.

At the National Institute of Standards and Technology (NIST), more than 40 research projects are addressing the semiconductor industry's immediate and looming measurement needs. This work spans the entire chipmaking process, from wafer characterization and device design to lithography and implantation to packaging and information flow across the engineering chain. In response to ITRS and input from International SEMATECH and other collaborators, NIST is intensifying its efforts to improve control of critical dimensions at the gate level; resolve issues associated with the use of complex gate stacks of metal and new low-k materials; and to develop "critical layer" metrology methods for detecting material incompatibilities, voids, "killer pores" and other defects that threaten interconnect reliability.

Researchers also are helping to pave the way for the mastery, introduction and integration of new types of materials and devices emerging from nanotechnology research. NIST's newly built Measurement Laboratory, which features a world's best combination of temperature, vibration and other environmental controls, will enable the institute and its partners to develop metrology as atomic lattice measurement references, and other supporting and fabrication capabilities necessary to move nanotechnology innovations out of the lab and into production.

Metrology

Christophe Fouquet
Director of Marketing, Negevtech



During the past few years, wafer fabs have continued to move toward 90 nm and on to 65 nm. There has even been some acceleration of this pace. The big red flag that should be evident at SEMICON West 2004 — is that 90 nm is where the complexities of process technology meet some really big challenges. For example, for several years there has been a lot of discussion about lithography, at least of which is the insertion of immersion and how it plays out with the extended range of 193 nm and the availability of 157 nm tools. It is still not clear what the lithography of the future is going to be. There are other areas of advanced processing that are as murky as lithography. Consider the technology paths of wafer inspection and metrology. In the past, with engineers developing production technology for the 90 and 65 nm nodes, in various ways there are real concerns that for the first time these development engineers do not have the inspection and metrology technologies in place at the start of their development work. Clear industry needs some breakthroughs that solve the natural limitations to conventional TDI C laser scanning inspection technology.

I believe that much of the buzz at SEMICON West this year is going to center on the stark difference between where we were at the start of developing 130 nm and where we are today. When first working on the development of 130 nm process technology, the engineers involved had a great idea of what technologies they would use. Today, moving beyond 130 nm, there are some significant unknowns. There are some real concerns that for the first time in some key areas equipment suppliers will not be able to develop the needed technology fast enough to meet fab demands.

Robert Loiterman

Senior Vice President of Technology and General Manager of Integrated Metrology Technologies



At SEMICON West this year, I expect to see a growing focus on inline inspection as a critical enabler of yield improvement. Yield has always been important. However, with today's more expensive wafers, new advanced materials and shorter product life cycles, the ability to quickly achieve and maintain the highest yields has become the determinant of success or failure. For this reason, the demand for inline inspection will continue to increase.

An excellent example is the inline detection of macrodefects — defects that are large relative to transistors or interconnect lines within ICs. These defects can affect multiple die or even the entire wafer, significantly impacting yield. If detected immediately after lithography — or to a lesser extent after CMP — processing, the affected wafer can generally be reworked and salvaged. It makes no sense to inspect every wafer because a fully processed 300 mm wafer can be worth tens of thousands of dollars. However, manual inspection is too slow and existing automated systems are too expensive to permit economical 100% inspection. Therefore, fabs inspect only a small fraction of their wafers. Macrodefect inspection is just one example of the growing need for inline inspection capabilities. This will enable process engineers to maximize yield, and ultimately profitability.

Jay Lindquist

Senior Vice President of Corporate Marketing, FEI Co.



With the convergence of shrinking devices and the growth of bottom-up, atom-by-atom, molecule-by-molecule fabrication applications, I believe we will hear a lot of talk about nanotechnology at SEMICON this year. Working with structures at the nanoscale is becoming an increasingly important focus for chipmakers today. Tools for thin-film heads and semiconductor devices require an understanding at that scale. For example, oxides, for example, are already only several molecules thick. As we approach the theoretical limits of conventional fabrication processes, scientists and engineers look more toward the promise of nanotechnology for new processes that will radically change the way we make microelectronic — or perhaps I should say nanoelectronic — devices. The shrinking dimensions of semiconductor devices — to the 90 nm node and below — require special tools that look at structures three-dimensionally. Not only are devices smaller, they are structurally more complex. The volume of features is as important as its "average" width. On this scale, the alignment of structures between layers is not trivial. Moreover, many of the processes used to create these structures are inherently three-dimensional, creating re-entrant features into previously deposited layers. They simply cannot be evaluated from a conventional top-down perspective.

The world is fundamentally different at the nanoscale. It requires new tools and new ways of thinking. FEI has been a part of much of that progress. Our tools are used today to help our customers understand what they are making in terms of size, structure, processes and materials. We hope that we can continue to contribute by delivering the tools for nanotech that the industry will forge ahead rapidly into the new "nano world."

Wasuke Nakano
COO, Hitachi High-Technologies Corp.



Unexpected error control is one of the biggest challenges in 45 nm node process. A common occurrence in 45 nm node processes is that the designed pattern on the reticle using phase shifting and/or optical proximity correction is different. Ideally, the pattern on the wafer is the same as the designed pattern. In practice, inaccuracies often occur during the process.

Hitachi High-Technologies addresses the challenges required of next-generation CD-SEM, and defect metrology equipment by developing systems with significant performance in phase control. Hardware and applications must be synchronized to enable complicated design architectures. Advanced device manufacturing requires highly accurate "measurement" of 2-D profiles, exact reticle measurement, and design verification by CD-SEM. Semiconductor device manufacturers call for low cost of ownership (CoO), which can be achieved through full auto high-throughput measurement and equipment uptime.

Future technology nodes (<65/45 nm) are increasingly confronted to produce void-free gap narrower features at the STI. The trench profile control and that of uniformity on the wafer are influenced parameters affecting yield and reliability.

Wafer cleaning/processing

Kurt Lackenbucher
Executive Vice President and Chief Marketing Officer, SEZ



Single-wafer processing, supplanting batch processing in the fab, is no longer an emergent trend — it's a given. Today, 70-80% of processing equipment is single-wafer technology. Cleaning remains the last frontier, but here, too, the trend is accelerating, driven most aggressively by Japan and Taiwan, where about 80% of cleaning equipment is single-wafer (vs. 20-25% worldwide).

One reason for the accelerated adoption is that the industry is moving from the 110 nm to 90 nm node, so more cleans are needed. Another factor is that memory device makers are now using single-wafer solutions; logic manufacturers adopted single-wafer cleaning more quickly because of the demands associated with copper interconnects.

Yield is the key factor behind the shift to single-wafer technology. The industry's yield issues at 90 nm and below can be addressed by introducing more single-wafer operations. At smaller geometries on 300 mm wafers, wafer value is too high; the risk of losing a whole wafer or an entire batch is significant. The technology provides the opportunity to produce the same number of chips per

smaller fab and less equipment.

Looking at the industry as a whole, I believe we'll be seeing far fewer joint ventures, joint development projects and other pursuits that deliver little return on investment. Because equipment makers must be more strategic about the markets we choose to enter and better able to stand on their own without joint projects.

Having said this, I'm optimistic about the current cycle, which is being extended by the need to replace under-capacity in a number of fabs. During the past two quarters, much equipment has been ordered and is currently being installed. This digestion period must be completed before new orders are placed, so the next wave of activity will begin in the second half of 2004, carrying the upcycle at least into 2005.

Scott Becker
Vice President of Marketing, FSI International



Over the past year, the semiconductor industry has experienced a very significant increase in factory utilization, while also struggling to improve yields on 90 nm technology. Prior to this upturn, factory utilization was low, and customers were interested in winning business by developing new technologies and reducing product-to-market cycle times.

To drive down cycle times, customers attempted to transition many of their batch processes to single-wafer platforms. In some instances, this proved effective at reducing cycle times, but it significantly increased capital costs and reduced overall fab capacity. To address these issues, we believe customers need to look at utilizing small-footprint batch processing tools. FSI has demonstrated the ability to reduce cycle times for critical cleans by >50% through innovative bench designs, and for BEOL cleans by >40% in batch tools using chemical processes or tools designed for single-wafer spray tools.

Simultaneously, customers continue to be challenged by yield goals in 90 nm manufacturing. Traditional brush scrubbers and megasonic energy have been effectively used for many years to achieve yield goals, but at 90 nm neither technique can be employed on mechanically sensitive structures such as exposed gate stacks and patterned low-k material. This has led to the development of brushless scrubbing and aerosol techniques. Water aerosols can be tuned to reduce damage, but this typically results in a 50% drop in particle removal efficiency. Hydrophobic materials such as SiN and OSG, used in copper/low-k interconnects, are particularly problematic because water-based cleaning techniques are ineffective (Sony Corp. presented very clear data on this at SEMICON Japan last December). We are now seeing unprecedented attention given to advanced techniques such as CryoKinetic cleaning, which is effective on both hydrophobic and hydrophilic surfaces without causing damage.

In summary, with factory utilization reaching its peak and IC makers experiencing an increase in demand for their products, conversation at SEMICON West 2004 will revert back to the traditional challenges of capital productivity and yield.

Emmanuel Turlot
CTO, Unaxis Wafer Processing



While 2004 is the first SEMICON West show in a long time that will have an economic message, the pace of technology innovation has continued at a fast pace over the past few years. Process innovations at Unaxis focus on both the silicon and compound semiconductor (non-silicon) technologies. For 2004, the process developments for Unaxis in the silicon technologies are:

- Mobile phone technology remains a key innovation driver. Processes for "above IC" of passives, filters and active films are being quickly industrialized to enable smaller energy-efficient and higher-frequency components
- Photomask technology is rapidly moving to the 65 nm node. With expected delivery of 45 nm node products only two years off, we anticipate significant movement in this area during the next 12 months.
- The flat-panel display boom has fueled huge demand for IC drivers for TFT panels. This has led to a large demand for wafer-level packaging solutions, particularly gold bumping.

Our developments for compound technology are:

- Applications for GaN continue to grow due to superior energy-to-light conversion efficiency, durability, especially for portable display and automotive applications (LED displays, automotive headlights and interior lighting). Further applications include general lighting and high-power RF devices.
- Use of SiGe technology keeps expanding — and taking market share from GaAs — due to better performance (high frequency and low noise) and integration capabilities for HEMT.

Equipment components and subsystems

Scott Sirignano
General Manager, Semiconductor Products, Poco Graphite



Hot topics will continue to be next-generation equipment that will support the advanced processes, but there is a growing interest in materials for key consumable components as these materials can help solve integration problems. Without continued development of these materials, next-generation equipment may not have the performance efficiencies necessary to lower costs.

We continue to see a push to drive design technologies from 130 nm to 90 nm. This trend has also affected the integration of both new processes and new materials in semiconductor manufacturing. As the integration of dual-damascene copper metallization, low-k dielectrics into these new geometries progresses, a number of critical issues have developed with some of the current consumable materials that support the equipment. Specifically, we are seeing a greater interest in silicon carbide chamber components as its attributes eliminate or reduce many of these issues that affect cost. Development of materials for consumable components is essential to improved performance and lower costs. SiC meets all the material performance needs for etch process and equipment. From a value standpoint, it has a much longer life than silicon, resulting in fewer preventive maintenance steps, which will lead to increased throughput and lower performance cost.

Steven Kirsch
Vice President, Pfeiffer Vacuum



Vacuum is, by definition, nothing. Yet this does not mean it should be taken granted. As fabs ramp back up to full capacity after a three-year lull, they are more challenges than ever. Uptime demands are increasing. Acceptable yield at all-time highs. Combine these pressures with smaller geometries, new ch and faster cycles times, and it is enough to keep even the most seasoned e engineer, tool owner or fab manager awake at night.

And yet, vacuum pumps — especially turbo pumps — are being treated more and more as commodity. While it may be true that turbo technology has progressed in recent years such most major suppliers' pumps can meet basic specs for most semi processes, this does not turbo pumps are created equal. It is one thing to meet pump down times and compression requirements, and quite another to do so consistently and reliably. Then there's a supplier's deliver on time, and to support its products immediately on a global basis. Only those companies can simultaneously manage these key aspects of their business will survive in the demand ahead.

Automation

Paul Sagues
President, Berkeley Process Control

Over the past several years, we have heard a lot about e-diagnostics. In an insightful recent Applied Materials' CEO Michael Splinter said in part, "If they have better diagnostics at the they'll fix it faster. The cost of service will go down. There will be a huge benefit there at that's, I think, the most critical and highest cost leverage." Mr. Splinter is telling us that we walk before we run. You can't have e-diagnostics until you have perfect local diagnostics.

Let's face it, today's semiconductor tools are too complex for the level of diagnostics providing relying too much upon highly skilled technicians, ready 24/7 to exercise good judgment and get tools back into production. This is not a sustainable model.

Our focus this year has been in wafer handling diagnostics. Now that we are able to automatically teach the wafer handling robots in both atmospheric and vacuum, we have moved to the next challenging problem: providing effective system-level diagnostics. Subtle mechanical or electrical defects can manifest themselves as bizarre problems. Recently, we saw a bad robot bearing itself as a wafer mapping error that led the tool builder to deduce that there was a problem FOUPL!

Diagnostics lacks the panache or sexiness that comes with e-diagnostics. After all, the visual diagnosing a problem over the Internet halfway around the world is pretty enticing. But I predict SEMICON this year, you will see more earthly visions presented. As Mr. Splinter points out be huge benefits.

Robert H. Reback
President and CEO, Cimatrix Inc.

Our view of the industry is, foremost, that of a supplier to wafer-fab tool OEMs. Being involved in tool automation, which is one of the industry's hot topics, and with more than 40 OEM customers, we have a broad overview of the industry's mood and what to expect at SEMICON West. Last year, the mood was still all about controlling costs and, frankly, survival. Equipment was not selling, software and connectivity needs had slowed considerably.

This year, based on the business activity that we have seen in the past six months, it is clear that we are in the midst of a solid recovery that has created short-term excitement and demand for tool automation solutions that will definitely be evident at SEMICON West. Today, OEMs are focused on tool delivery, but many top-tier OEMs are in the middle of designing new software architectures aimed at improving the reliability of their factory automation software and preparing new interfaces to support APC applications.

Because our software ships in OEM tools, we know that equipment shipments are up significantly. Earlier this year, Cimatrix announced its first profitable quarter since the downturn began. Demand has clearly improved, and this will be reflected at SEMICON West 2004. Overall, it is a good sign for the semiconductor industry. But this is still a cyclical industry, so everyone will probably be asking, "How long do you think the recovery will last?"

Adrian Fuchser
Executive Vice President and General Manager, Schneeberger Inc.

Moore's Law has been accurate for more than 30 years now. Over time, some experts believe that certain physical barriers had been penetrated and Moore's Law could be compromised. Yet today, Moore's Law stands true and miniaturization, higher density and smaller structures will continue to be the major technology drivers impacting the semiconductor industry and, in parallel, the velocity of linear motion.

The process of creating a chip requires a certain caliber of linear motion and hence, the requirements for linear positioning systems are considerably on the rise. Such positioning is often used in conjunction with yield improvement tools in several processes, including inspection.

Because inspection tools have advanced faster than the rest of the semiconductor equipment industry, it has enabled chipmakers to increase the yield of a fab and receive higher throughput without investing in additional, more expensive capacity.

Merely optical magnification is not enough to verify tiny conductors, thus electron-beam microscopy and other technologies are used and are capable of delivering the required resolution. Nevertheless, before any verification can be performed, the wafer needs to be moved to the exact position where the microscope can verify the tiny conductor. Consequently, the smaller structures on wafers require higher precision of motion systems. Or, once the accurate location is found, the motion system has to stand still and not jitter. A standard motion system will always move between the encoded position increments. By pushing the physical limits and being able to achieve sub-nanometer resolution with position feedback, it is still possible to control the loop beyond the resolution of the microscope. In a wafer scanning application, the requirements on velocity ripple become extremely demanding to read each sub-nanometer pixel precisely.

Although there are many other examples that could be mentioned, it is evident that the challenge does not only lie in the hands of the equipment builders, but also with the co-developers and supplier subsystems — in this case on motion technology. A supplier of such solutions must have comprehensive and profound understanding of these types of challenges.

Robert Deuster
Chairman and CEO, Newport Corp.

Our industry is recovering from a three-year downturn, which has resulted in a somewhat a supply chain. As demand now increases, companies throughout the industry are striving to Therefore, a key component in the future for rapid response will be the development and de technologies to reduce lead times, and a greater focus on operational excellence at compa throughout the industry.

Part of the total lead time improvement for our customers translates into high-yield process metrology equipment that can be installed and configured in minimum time, and operated v extensive, machine-specific operator training. Ease of use and reliable advanced technolog enable users to readily achieve the equipment throughput numbers specified by the vendor Performix EFEM, which features an automated self-teach wafer handling robot, for example inherent repeatability that enables even inexperienced operators to achieve benchmark thr with very minimal training.

Operationally, suppliers throughout the industry will need to respond with sufficient capacit up with increasing demand. At Newport, we will triple our capacity to build wafer automatio equipment by the end of 2004. However, because of continual price and competitive pressu market, we will need to do that in a much smarter way. Manufacturers such as ourselves w stay focused on increasing productivity everywhere in our own supply chain. For example, we utilize online work instructions for our ADO load port product line. This enables rapid de and scaling of labor to easily flex with the changing demand environment and produces les dependence on highly skilled personnel.

Often, when industry leaders, analysts and pundits discuss technical trends at an industry such as SEMICON West, the emphasis is on breakthrough technologies that will enable ir roadmaps to be followed. But this year presents a different proposition; the real story relate business agility. Specifically, it's about the operational and technological tools that facilitat delivery times.

Equipment strategies

Cathy Edgington
**Market Development Manager, Semiconductor/Aerospace Performance Plastics Pr
(3P)**

Nanotechnology in tandem with material design will be of significant interest at SEMICON With the acceleration of the business climate, the demand for new, innovative and competii materials continues in the semiconductor market. There are new applications and new tecl emerging almost weekly requiring materials not yet invented, or just now beginning to garn by an entire industry.

As this industry matures, the race is on for new polymeric materials to replace the old star areas of conductivity, electrostatic dissipation and chemical compatibility. High purity and l temperature tolerance is an old requirement, but with new twists, thus the value of high-per plastics becomes an even more desirable alternative to metallic materials in the process lc Nano-composites are coming of age and are enabled through the most recent developmen created on a nanoscale. New process equipment designs will benefit from this technology :

incorporate it into initial prototypes as they are launched in the coming months.

Whether new applications have high or low volume potential is not the ultimate driver of this technology. It is the engineering of the material blend itself that will be the key to unlocking solution for niches of the semiconductor market that have not yet been elucidated.

Jeffrey P. Sercel
President, JPSA Laser

Scribing with UV diode-pumped solid-state (DPSS) lasers will continue to gain popularity as an alternative method of scribing semiconductor wafers for separation, particularly for thin silicium germanium wafers, as well as other brittle compound semiconductor wafers materials such as GaAs. This method is not only preferable to mechanical scribing, but also better than conventional laser scribing, whereby a simple far-field imaging technique is used. The primary benefit with this approach is that the focused beam spot in the conventional far-field imaging does not have sufficient flexibility to adjust for optimum intensity, which is determined by the light absorption properties of a particular target.

Recently, frequency-multiplied DPSS lasers have demonstrated significant improvements in pulse duration, frequency and power output. A focused beam spot with short pulse duration creates extremely high irradiance, resulting in instantaneous vaporization of materials during wafer scribing.

With UV-DPSS laser systems, we're now seeing high-speed blue LED wafer scribing with yields >99% at less than \$2 per wafer. This process cuts a well-defined, square chip, with consistently narrow cuts as small as 5 µm. With its high throughput — up to 8 wph — and minimal impact on LED performance, the process is tolerant of wafer warp and bow, and delivers a scribing speed compared with mechanical scribing. The DPSS laser process provides a 500% increase in throughput, with a 97.5% reduction in operating costs.

Trey Brown
General Manager, GE Commercial Finance, Global Electronics Solutions

For all the efficiency benefits that 300 mm fabrication brings to semiconductor manufacturing, equipment costs are delaying mainstream deployment. The price tag to build and equip 30 manufacturing facilities is nearly \$3B, with almost 80% devoted to capital equipment.

To make money, manufacturers need to tightly manage their equipment costs, with an eye on positioning themselves to take full advantage of the oncoming upturn. That is why many semiconductor manufacturers are forming external strategic relationships with a new breed of semiconductor-savvy financial organizations. These third-party companies offer an in-depth understanding of technology trends with a full range of leasing, purchasing, sales/leaseback, equipment evaluation/locator services.

The synthesis of technical, capital and financial expertise offers the critical mass semiconductor manufacturers a way to achieve a financially sound approach for migrating to 300 mm. The partners can help semiconductor companies evaluate the various different approaches for a 300 mm equipment while taking into account the long-term requirements of equipment optimization and eventual disposition.

At each stage of the 300 mm equipment lifecycle, the financial organizations can assist semiconductor manufacturers in managing the risk of their capital equipment. Some offer s

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financial resources and an array of financing options during the crucial acquisition phase for equipment. Then they can help manufacturers develop a long-term strategy to ensure the cost over the effective lifetime of the equipment. Finally, when the time comes to replace and upgrade equipment, the external partner can act as a qualified intermediary, providing comprehensive remarketing services.

Semiconductor manufacturers are finding that relying on the financial and technical resources of third-party organizations can help them successfully negotiate the transition to 300 mm wafers while minimizing both the short-term and long-term risks.

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